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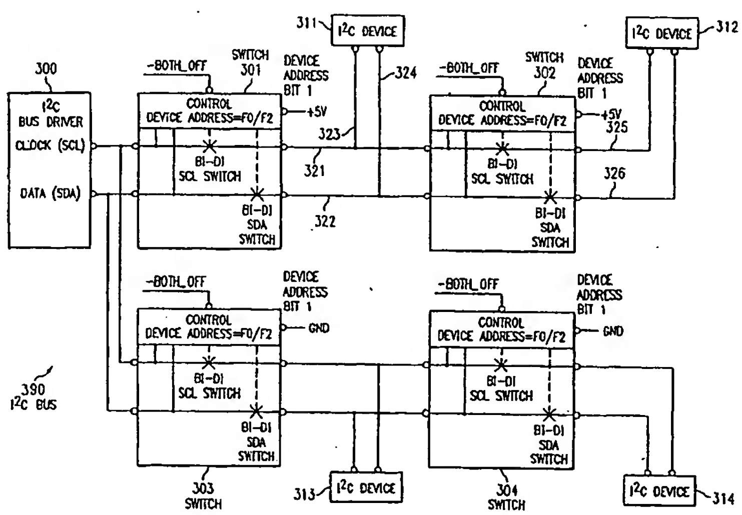
(54) Title: I2C SELF BUS SWITCHING DEVICE



(57) Abstract: A bus switch module for use in a bus such as an I²C bus is provided. In one embodiment, the switch module includes a control unit and a switch. The control unit includes an input for receiving instructions from a bus driver as to whether to close or open the switch. The switch includes a first and a second data connection which connect the switch to a first and a second segment of the bus and includes a control input for receiving commands from the control unit. The control unit opens and closes the switch in response to instructions received from the bus driver and signals received in the first data connection are passed to the second data connection only when the switch is closed in response to a command from the control unit. Thus, the bus switch module allows a bus driver to isolate devices and switch modules connected in series by opening or closing the switch.

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I²C SELF BUS SWITCHING DEVICE

BACKGROUND OF THE INVENTION

Technical Field

The present invention relates to computer bus architecture. More specifically, the present invention relates to Inter Integrated Circuit (I²C) buses.

Description of Related Art

Many similarities exist between seemingly unrelated designs in consumer, industrial and telecommunication electronics. Examples of similarities include intelligent control, general-purpose circuits (i.e. LCD drivers, I/O ports, RAM) and application-oriented circuits. The Philips Inter Integrated Circuit (I²C) bus is a bi-directional two-wire serial bus designed to exploit these similarities.

Devices on the I²C bus are accessed by individual addresses, 00-FF (even addresses for Writes, odd addresses for reads). The I²C architecture can be used for a variety of functions. One example is Vital Product Data (VPD). Each component in the system contains a small Electrically Erasable Programmable Read Only Memory (EEPROM) (typically 256 bytes) which contains the VPD information such as serial numbers, part numbers, and EC revision level.

I²C busses can connect a number of devices simultaneously to the same pair of bus wires. However, a problem results when one of the devices malfunctions and pulls a bus signal (clock or data) low. The bus will not operate and it is very difficult to determine which of the numerous devices connected to the I²C bus is responsible. A similar problem occurs when one of the bus conductors becomes shorted to a low impedance source, such as, for example, ground.

SUMMARY OF THE INVENTION

Accordingly, the invention provides a bus switch module, comprising: a control unit with an input for receiving instructions from a bus driver; and a switch with a first and a second data connection which connect the switch to a first and a second segment of a bus; wherein the control unit opens and closes the switch in response to instructions received from the.

bus driver; and signals received in the first data connection are passed to the second data connection only when the switch is closed.

Preferably an improved I^2C bus is provided from which it is readily determinable the device that has malfunctioned resulting in the bus ceasing to operate.

The present invention preferably provides a bus switch module for use in a bus such as an I^2C bus. In one embodiment, the switch module includes a control unit and a switch. The control unit preferably includes an input for receiving instructions from a bus driver as to whether to close or open the switch. The switch preferably includes a first and a second data connection which connect the switch to a first and a second segment of the bus and includes a control input for receiving commands from the control unit. In a preferred embodiment the control unit opens and closes the switch in response to instructions received from the bus driver and signals received in the first data connection are passed to the second data connection preferably only when the switch is closed in response to a command from the control unit. Thus, the bus switch module allows a bus driver to isolate devices and switch modules connected in series by opening or closing the switch.

In a preferred embodiment, the bus switch module is a bi-directional switch capable of passing signals received at the second data connection to the first data connection and of passing signals received at the first data connection to the second data connection only when the switch is closed.

Preferably the switch is a first switch and the signals are first signals. In a preferred embodiment, the bus switch module further comprises a second switch with a third and a fourth data connection which connect the switch to a third and a fourth segment of the bus. Preferably the control unit opens and closes the second switch in response to instructions received from the bus driver and second signals received in the third data connection are passed to the fourth data connection only when the switch is closed.

In a preferred embodiment, the second switch is a bi-directional switch capable of passing signals received at the fourth data connection to the third data connection and of passing signals received at the third data connection to the fourth data connection only when the second switch is closed.

Preferably the switch is a clock switch for passing clock signals only when the clock switch is closed.

In a preferred embodiment the switch is a data switch for passing data signals only when the data switch is closed.

Preferably, the first switch is a clock switch for passing clock signals only when the clock switch is closed and the second switch is a data switch for passing data signals only when the data switch is closed.

In a preferred embodiment, the bus is an inter integrated circuit bus.

Preferably the control unit includes a reset input and a reset module which, in response to receiving a reset signal from the bus driver, opens both switches.

According to one embodiment, the invention provides a bus for use in connecting electronic components, comprising: a bus driver; and a plurality of bus switch modules each connected by a plurality of bus lanes with at least one of the plurality bus switch modules connected to the bus driver; wherein each of the plurality of bus switch modules comprises: a control unit with an input for receiving instructions from a bus driver; and a switch with a first and a second data connection which connect the switch to a first and a second segment of a bus; wherein the control unit opens and closes the switch in response to instructions received from the bus driver; and signals received in the first data connection are passed to the second data connection only when the switch is closed.

According to one embodiment, the invention provides a data processing system, comprising: a plurality of components; a bus communicably coupling the plurality of components wherein the bus comprises: a bus driver; and a plurality of bus switch modules each connected by a plurality of bus lanes with at least one of the plurality bus switch modules connected to the bus driver; wherein each of the plurality of bus switch modules comprises: a control unit with an input for receiving instructions from a bus driver; and a switch with a first and a second data connection which connect the switch to a first and a second segment of a bus; wherein the control unit opens and closes the switch in response to instructions received from the bus driver; and signals received in the first data connection are passed to the second data connection only when the switch is closed.

BRIEF DESCRIPTION OF THE DRAWINGS

A preferred embodiment of the present invention will now be described by way of example only and with reference to the following drawings:

Figure 1 depicts a pictorial representation of a data processing system in which a preferred embodiment of the present invention is implemented;

Figure 2 depicts a block diagram of a data processing system in which a preferred embodiment of the present invention is implemented;

Figure 3 depicts a schematic diagram illustrating a I^2C self bus switching device in accordance with a preferred embodiment of the present invention; and

Figure 4 depicts a block diagram of an I^2C bi-directional bus switch module in accordance with a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

With reference now to the figures and in particular with reference to Figure 1, a pictorial representation of a data processing system in which a preferred embodiment of the present invention is implemented is depicted. A computer 100 is depicted which includes a system unit 110, a video display terminal 102, a keyboard 104, storage devices 108, which may include floppy drives and other types of permanent and removable storage media, and mouse 106. Additional input devices may be included with personal computer 100, such as, for example, a joystick, touchpad, touch screen, trackball, microphone, and the like. Computer 100 can be implemented using any suitable computer, such as an IBM RS/6000® computer or IntelliStation® computer, which are products of International Business Machines Corporation, located in Armonk, New York. Although the depicted representation shows a computer, other embodiments of the present invention may be implemented in other types of data processing systems, such as a network computer. Computer 100 also preferably includes a graphical user interface that may be implemented by means of systems software residing in computer readable media in operation within computer 100.

With reference now to Figure 2, a block diagram of a data processing system is shown in which a preferred embodiment of the present invention

is implemented. Data processing system 200 is an example of a computer, such as computer 100 in Figure 1, in which code or instructions implementing the processes of the preferred embodiment may be located. Data processing system 200 employs an I^2C bus architecture. The I^2C bus 248 is a bi-directional serial bus requiring only two wires: a serial data line (SDA) and a serial clock line (SCL). Although serial buses do not have the throughput capability of parallel buses, serial buses require less wiring and fewer Integrated Circuit (IC) connector pins. Each device (processor 202, electronically erasable and programmable read only memory (EEPROM) 240, temperature sensor 242, and any other I^2C device 244) connected to I^2C bus 248 is software addressable by a unique address. The devices can operate as either transmitters or receivers. All I^2C bus compatible devices have an on-chip interface which allows the devices to communicate directly with each other via the I^2C bus 248. A simple master/slave relationship exists at all times. A master is a device which initiates a data transfer and the clock signals to permit the transfer, and any device addressed at the time of transfer is considered a slave. The I^2C bus is a multimaster bus, meaning more than one device capable of controlling the bus can be connected to it. However, the preferred embodiment is operated in a single-master mode. Typical I^2C local bus implementations will support three or four I^2C expansion slots or add-in connectors.

Processor 202 and main memory 204 are connected to PCI local bus 206 through PCI bridge 208. PCI bridge 208 also may include an integrated memory controller and cache memory for processor 202. Additional connections to PCI local bus 206 may be made through direct component interconnection or through add-in boards. In the depicted example, local area network (LAN) adapter 210, small computer system interface SCSI host bus adapter 212, and expansion bus interface 214 are connected to local bus 206 by direct component connection. In contrast, audio adapter 216, graphics adapter 218, and audio/video adapter 219 are connected to local bus 206 by add-in boards inserted into expansion slots. Expansion bus interface 214 provides a connection for a keyboard and mouse adapter 220, modem 222, and additional memory 224. SCSI host bus adapter 212 provides a connection for hard disk drive 226, tape drive 228, and CD-ROM drive 230.

An operating system runs on processor 202 and is used to coordinate and provide control of various components within data processing system 200 in Figure 2. The operating system may be a commercially available operating system such as Windows® 2000, which is available from Microsoft®

Corporation (Windows and Microsoft are registered trademarks of Microsoft Corporation in the United States and/or other countries). An object oriented programming system such as Java™ may run in conjunction with the operating system and provides calls to the operating system from Java programs or applications executing on data processing system 200. "Java" is a trademark of Sun Microsystems, Inc. Instructions for the operating system, the object-oriented programming system, and applications or programs are located on storage devices, such as hard disk drive 226, and may be loaded into main memory 204 for execution by processor 202.

Those of ordinary skill in the art will appreciate that the hardware in Figure 2 may vary depending on the implementation. Other internal hardware or peripheral devices, such as flash ROM (or equivalent nonvolatile memory) or optical disk drives and the like, may be used in addition to or in place of the hardware depicted in Figure 2. Also, the processes of the preferred embodiment may be applied to a multiprocessor data processing system.

For example, data processing system 200, if optionally configured as a network computer, may not include SCSI host bus adapter 212, hard disk drive 226, tape drive 228, and CD-ROM 230, as noted by dotted line 232 in Figure 2 denoting optional inclusion. In that case, the computer, to be properly called a client computer, preferably includes some type of network communication interface, such as LAN adapter 210, modem 222, or the like. As another example, data processing system 200 may be a stand-alone system configured to be bootable without relying on some type of network communication interface, whether or not data processing system 200 comprises some type of network communication interface. As a further example, data processing system 200 may be a personal digital assistant (PDA), which is configured with ROM and/or flash ROM to provide non-volatile memory for storing operating system files and/or user-generated data.

The depicted example in Figure 2 and above-described examples are not meant to imply architectural limitations. For example, data processing system 200 also may be a notebook computer or hand held computer in addition to taking the form of a PDA. Data processing system 200 also may be a kiosk or a Web appliance.

The processes of the preferred embodiment are performed by processor 202 using computer implemented instructions, which may be located in a

memory such as, for example, main memory 204, memory 224, or in one or more peripheral devices 226-230.

I^2C buses can connect a number of devices simultaneously to the same pair of bus wires. However, a problem results when one of the devices malfunctions and pulls a bus signal (clock or data) low. The I^2C bus will not operate in this situation, and it is difficult to determine which device is causing the problem. A similar problem occurs when one of the I^2C bus conductors becomes shorted to a low impedance source, such as ground. The solution to these problems is to break the bus into sections in order to determine which section contains the fault. This can be accomplished with the I^2C self bus switching device.

The I^2C self bus switching device monitors the I^2C bus and responds to its own address. The device also passes bus signals through if its switches are turned on. "On" means that the circuit is closed (i.e. the devices downstream from the switch will be connected to the bus and can see the bus traffic). When the switch is "off", the downstream devices are disconnected from the bus. The device can be commanded to turn its switches on or off, and the switches can also be turned off independent of the I^2C bus by the switch reset signal. An eight-pin package, for example, permits one address bit to be programmed. This allows switch devices to deal with a bus that has a forked path. A larger pin package can have more address options.

Referring now to Figure 3, a schematic diagram illustrating a I^2C self bus switching device is depicted in accordance with a preferred embodiment of the present invention. I^2C bus 390 may be implemented as, for example, I^2C bus 248 in Figure 2. The bus driver 300 can communicate with the four main devices 311-314, plus switches 301-304. If a fault occurs on the I^2C bus, the system will assert a signal to reset all of the switches 301-304. The bus master will send a bus command on a predefined address to indicate that switch 301 should turn on. Since only switch 301 can see this command (switch 302 is disconnected), switch 301 operates but switch 302 does not, since the off condition of switch 301 prevented switch 302 from seeing the command. This switch-on command connects the device 311 and switch 302 to the bus. If a fault now exists, it is located in device 311, switch 302, or on the bus connectors 321-324 just switched on.

If no fault exists, the bus master can once again send a command to the predefined address. Both switches 301 and 302 will see this command,

but switch 301 will not change its switch status since it is already on. Switch 302 will respond to the command, and will then connect device 312 to the bus. If a fault occurs, it is located in device 312 or on the bus connectors 325 and 326. This process is continued with the switches 303 and 304 and devices 313 and 314. In this example, switches 301 and 303 are connected in parallel, but switch 303 has an address bit pulled down, which makes its predefined address different from that of switch 301.

Although the switches have been described herein as either separate chips or incorporated into the I^2C bus itself, the switches could also be incorporated into one of the devices connected to the I^2C bus. Furthermore, the switch could be incorporated into an existing switch on an I^2C device with separate signals and/or commands to indicate which switching function that the switch should perform. Thus, the present invention is not limited to the specific embodiment described herein.

With reference now to Figure 4, a block diagram of an I^2C bi-directional bus switch module is depicted in accordance with a preferred embodiment of the present invention. I^2C bi-directional bus switch module 400 may be implemented as, for example, any of switches 301-304 in Figure 3. In the depicted example, switch module 400 is an eight pin 404-418 package that includes control unit 402 and switches 420-422. For clarity, not all connections, such as power connections, within switch module 400 are shown.

Pin 404 is a voltage input pin connected, in one embodiment, to a 5 volt power source. Pin 412 is connected to ground. Control unit 402 will respond to a predefined address, one bit of which is determined by pin 418 being pulled high or low. Thus, the bus driver may direct certain data or instructions to a particular switch module.

Pin 416 receives clock signals from a bus driver and passes these signals to control unit 402 as well as to clock signal switch 422. Clock signal switch 422 can be closed or opened by control unit 402 as directed by a bus driver. If clock signal switch 422 is open, any clock signals received via pin 416 are prevented from being sent to downstream switch modules or devices. If clock signal switch 422 is closed, then any clock signal received via pin 416 is still received by control unit 402 but in addition, the signal is passed downstream to other switch modules and/or devices via pin 414. Clock signal switch 422 may also receive signals from pin 414 which may be passed to control unit 402 as well as upstream to other switch modules, devices, and/or the bus driver via pin 416 if

clock signal switch 422 is closed and are prevented from being passed upstream if clock signal switch 422 is open.

Pin 408 receives data signals from a bus driver and passes these data signals to both the control unit 402 and data signal switch 420. If control unit 402 has been instructed by the bus driver to close data signal switch 420, then data signals received via pin 408 are still received by control unit 402 but in addition, the signals are passed downstream to other switch modules and/or devices by data signal switch 420 via pin 410. If control unit 402 has been instructed by the bus driver to open data signal switch 420, then data signals received via pin 408 are prevented from being passed downstream by data signal switch 420. Similarly, any data signals received from downstream by data signal switch 420 via pin 410 are passed or prevented from being passed upstream to other switch modules, devices, and/or the bus driver depending on whether data signal switch 420 has been closed or opened by control unit 402.

Switch module 400 also includes a pin 406 which receives switch reset signals from the bus driver and passes these signals to control unit 402. If a switch reset signal is received by control unit 402, both switches 420-422 are opened. By doing this, the bus driver can reset all switch modules at once in response to a malfunctioning device or switch module that has caused the I^2C bus cease functioning properly and then determine which of the devices has caused the problem by selectively turning on switch modules until the malfunctioning device or switch is found.

The bi-directional bus switch module depicted herein is given merely by way of example and is not intended as an architectural limitation to the present invention. Other embodiments of a bus switch may, for example, include different numbers of pins and include other components not shown.

CLAIMS

1. A bus switch module, comprising:

a control unit with an input for receiving instructions from a bus driver; and

a switch with a first and a second data connection which connect the switch to a first and a second segment of a bus; wherein

the control unit opens and closes the switch in response to instructions received from the bus driver; and

signals received in the first data connection are passed to the second data connection only when the switch is closed.

2. The bus switch module as recited in claim 1, wherein the switch is a bi-directional switch capable of passing signals received at the second data connection to the first data connection and of passing signals received at the first data connection to the second data connection only when the switch is closed.

3. The bus switch module as recited in claim 1, wherein the switch is a first switch and the signals are first signals, further comprising:

a second switch with a third and a fourth data connection which connect the switch to a third and a fourth segment of the bus; wherein

the control unit opens and closes the second switch in response to instructions received from the bus driver; and

second signals received in the third data connection are passed to the fourth data connection only when the switch is closed.

4. The bus switch module as recited in claim 3, wherein the second switch is a bi-directional switch capable of passing signals received at the fourth data connection to the third data connection and of passing signals received at the third data connection to the fourth data connection only when the second switch is closed.

5. The bus switch module as recited in claim 1, wherein the switch is a clock switch for passing clock signals only when the clock switch is closed.

6. The bus switch module as recited in claim 1, wherein the switch is a data switch for passing data signals only when the data switch is closed.

7. The bus switch module as recited in claim 3, wherein the first switch is a clock switch for passing clock signals only when the clock switch is closed and the second switch is a data switch for passing data signals only when the data switch is closed.

8. The bus switch module as recited in claim 1, wherein the bus is an inter integrated circuit bus.

9. The bus switch module as recited in claim 1, wherein the control unit includes a reset input and a reset module which, in response to receiving a reset signal from the bus driver, opens both switches.

10. A bus for use in connecting electronic components, comprising:

a bus driver; and

a plurality of bus switch modules each as claimed in any of claims 1 to 9 and each connected by a plurality of bus lanes with at least one of the plurality bus switch modules connected to the bus driver.

11. A data processing system, comprising:

a plurality of components; and

a bus as claimed in claim 10 communicably coupling the plurality of components.

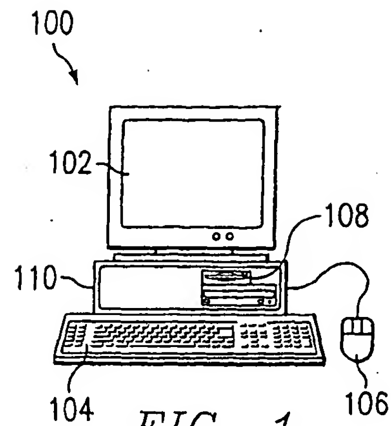

100
102
108
110
104
106

FIG. 1

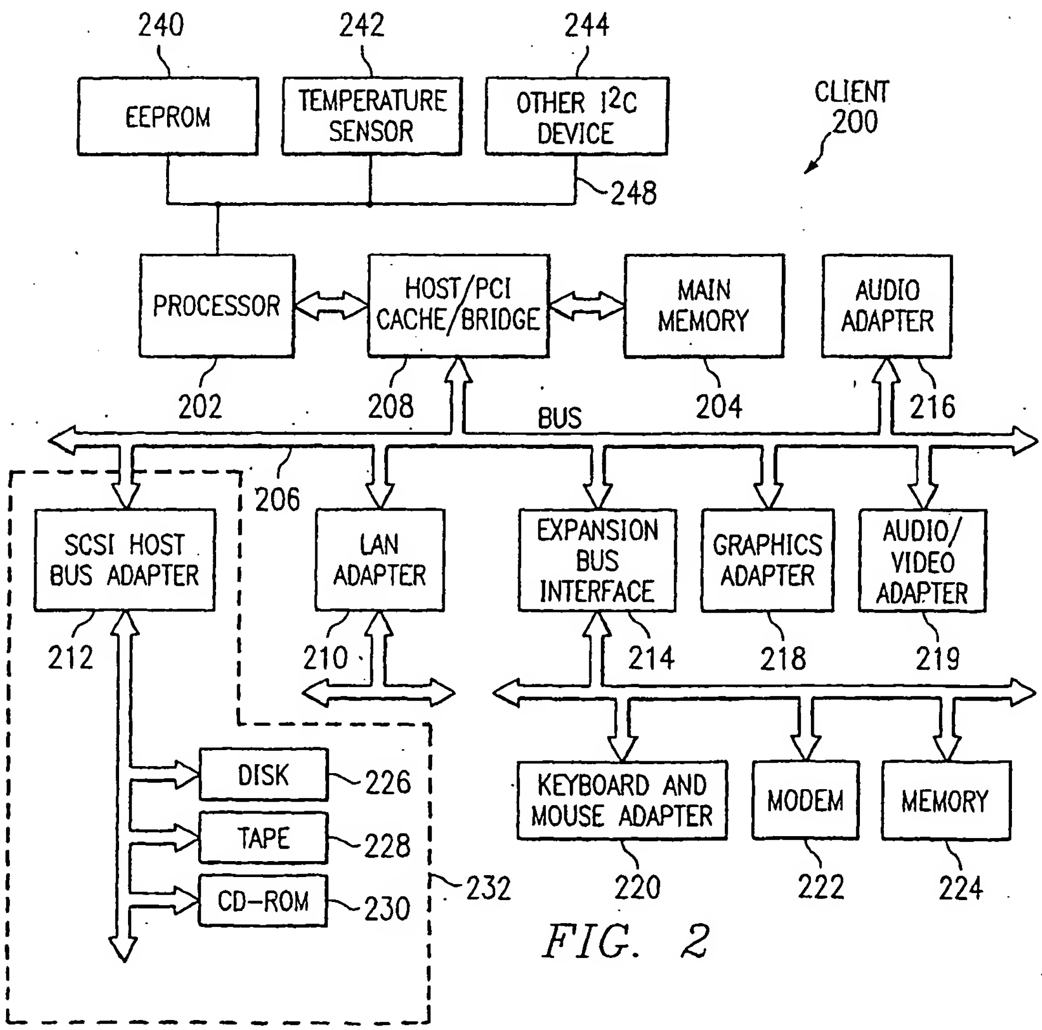
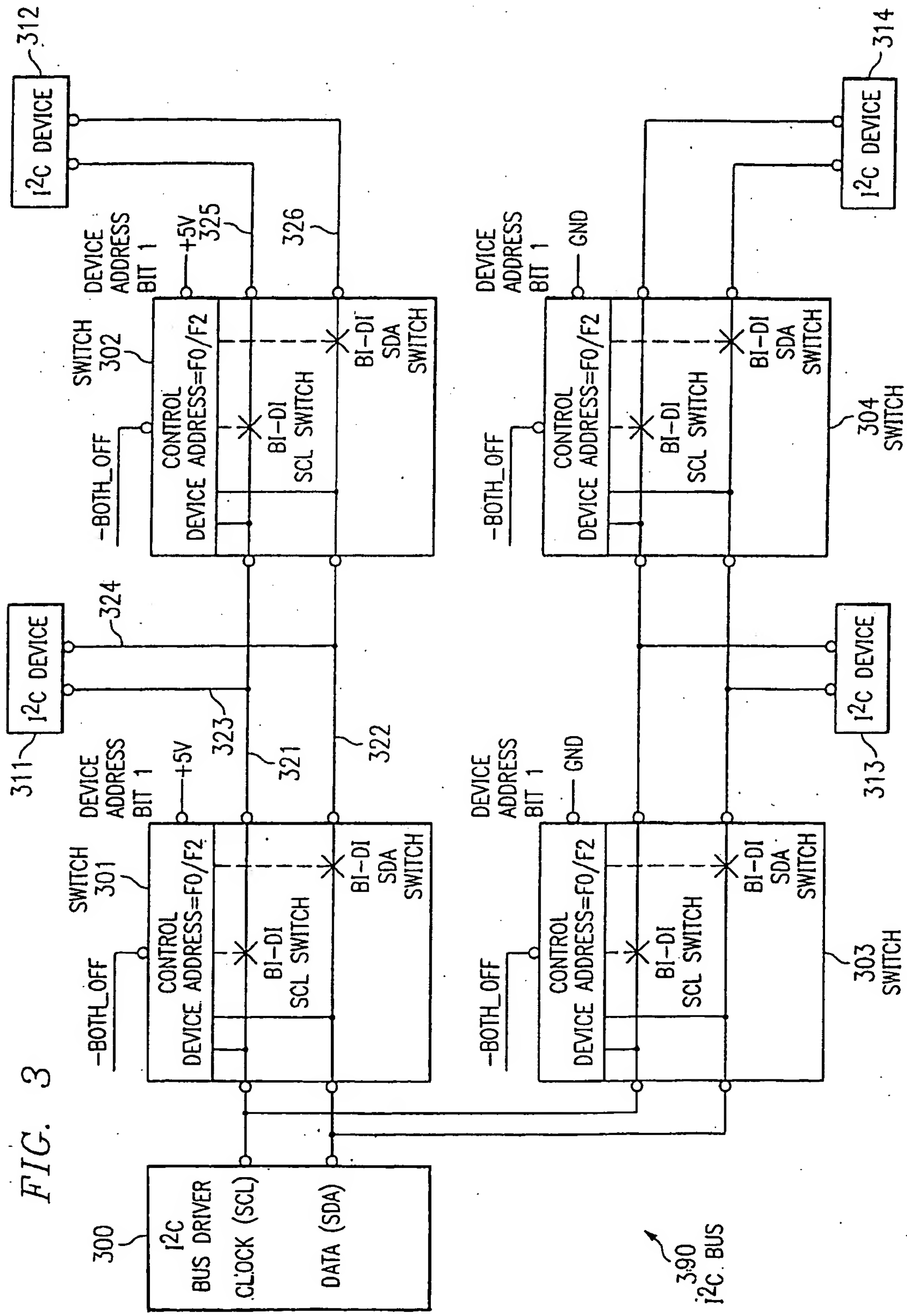

240
242
244
EEPROM
TEMPERATURE SENSOR
OTHER I2C DEVICE
CLIENT 200
248
PROCESSOR
HOST/PCI CACHE/BRIDGE
MAIN MEMORY
AUDIO ADAPTER
202
208
204
216
BUS
206
SCSI HOST BUS ADAPTER
LAN ADAPTER
EXPANSION BUS INTERFACE
GRAPHICS ADAPTER
AUDIO/ VIDEO ADAPTER
212
210
214
218
219
DISK
226
TAPE
228
CD-ROM
230
232
KEYBOARD AND MOUSE ADAPTER
MODEM
MEMORY
220
222
224

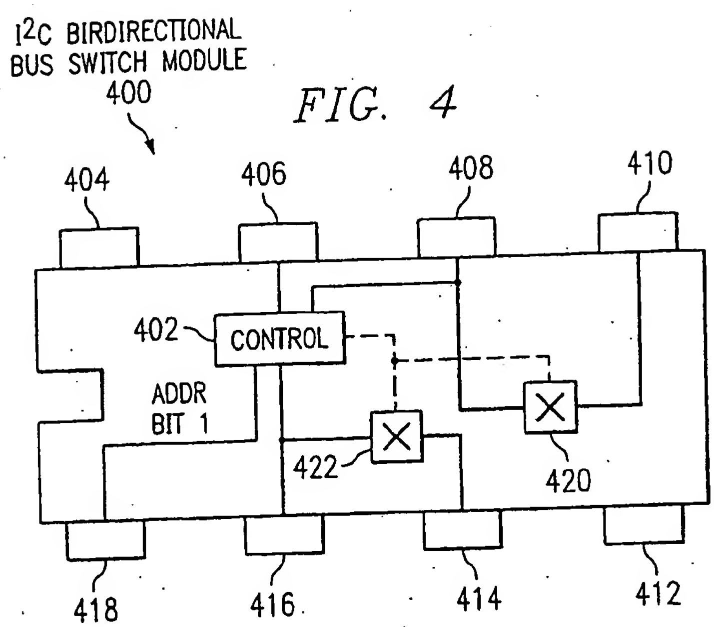
FIG. 2



I²C DEVICE
312
314
DEVICE ADDRESS BIT 1
+5V
325
326
GND
SWITCH 302
CONTROL DEVICE ADDRESS=F0/F2
BI-DI SCL SWITCH
BI-DI SDA SWITCH
-BOTH_OFF
304 SWITCH
324
323
311
321
322
313
SWITCH 301
303 SWITCH
300
I²C BUS DRIVER
CLOCK (SCL)
DATA (SDA)
390 I²C BUS

FIG. 3

FIG. 4


I2C BIRDIRECTIONAL
BUS SWITCH MODULE
400
404
406
408
410
402
CONTROL
ADDR
BIT 1
422
420
418
416
414
412